

SYNCHRONIZING DATA OR SIGNAL TRANSFER ACROSS CLOCKED LOGIC DOMAINS

Abstract of the Disclosure

5 A synchronization interface transfers multi-bit digital data or signal between
multiple clocked logic domains while maintaining data or signal integrity. When
deployed in a processor-based system, in one embodiment, a plurality of data units may
be received at a source location in a first clocked domain. To control writing of the
plurality of data units from the source location to a target location in a second clocked
domain, an enable signal may be detected. This enable signal may be synchronized with
10 respect to the second clocked domain. Finally, in response to the synchronized enable
signal, the plurality of data units may be transferred from the first clocked domain to the
target location in the second clocked domain. The synchronization interface may
comprise a data path to capture the multi-bit digital data or signal based on a control logic
implementing a mechanism (e.g., a state machine) to synchronously transfer the data
15 across a first and a second asynchronously clocked domains capable of receiving a first
and a second clock, respectively.